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EXAMINER	
MILORD, MARCEAU	
ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/692,420	Applicant(s) DARABI ET AL.	
	Examiner Marceau Milord	Art Unit 2682	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 October 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-81* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-81* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 October 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. Claim 62 is objected to because of the following informalities: In claim 62, line 24; "a period " should be placed after the word resistor. Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-61, 75-81 are rejected under 35 U.S.C. 102(e) as being anticipated by Vorenkamp et al (US Patent No 6591091 B1).

Regarding claim 1, Vorenkamp et al discloses a filter circuit (fig. 5 and fig. 19), comprising: a plurality of cascaded filters (510, 512 of fig. 5; col. 11, line 25-47; col. 27, lines 31-55); and a bypass circuit coupled across one of the cascaded filters (col. 11, lines 10-65; col. 12, lines 7-5; col. 27, line 48- col. 28, line 67).

Regarding claim 2, Vorenkamp et al discloses a filter circuit (fig. 5), comprising: a plurality of cascaded filters (510, 512 of fig. 5); wherein the bypass circuit comprises a switch (col. 11, lines 10-65).

Regarding claim 3, Vorenkamp et al discloses a filter circuit (fig. 5), comprising: a plurality of cascaded filters (510, 512 of fig. 5); further comprising a plurality of bypass circuits including the bypass circuit, the bypass circuit each being coupled across a different none of the cascaded filters (col. 11, lines 10-65; col. 12, lines 7-5; col. 27, line 48- col. 28, line 67).

Regarding claim 4, Vorenkamp et al discloses a filter circuit (fig. 5), comprising: a plurality of cascaded filters (510, 512 of fig. 5); wherein each of the bypass circuits are adapted for individual control (col. 13, lines 21-65).

Regarding claim 5, Vorenkamp et al discloses a filter circuit (fig. 5), comprising: a plurality of cascaded filters (510, 512 of fig. 5); wherein the bypass circuits each comprises a switch (col. 11, lines 10-65).

Regarding claim 6, Vorenkamp et al discloses a filter circuit (fig. 5), comprising: a plurality of cascaded filters (510, 512 of fig. 5); wherein the cascaded filters each comprises a biquad filter (510, 512 of fig. 5; col. 11, line 25-47; col. 27, lines 31-55).

Regarding claim 7, Vorenkamp et al discloses a filter circuit (fig. 5), comprising: a plurality of cascaded filters (510, 512 of fig. 5); wherein, the cascaded filters each comprises a complex filter (col. 13,line 8- col. 14, line 62).

Regarding claim 8, Vorenkamp et al discloses a filter circuit (fig. 5), comprising: a plurality of cascaded filters (510, 512 of fig. 5); wherein the cascaded filters each comprises a differential filter (col. 13,line 8- col. 14, line 62).

Regarding claim 9,Vorenkamp et al discloses a filter circuit (fig. 5), comprising: a plurality of cascaded filters (510, 512 of fig. 5); wherein the cascaded filters each comprises a pole and a zero (col. 13,line 8- col. 14, line 62; col. 12, lines 7-51; col 14, lines 1-62).

Regarding claim 10,Vorenkamp et al discloses a filter circuit (fig. 5), comprising: a plurality of cascaded filters (510, 512 of fig. 5); wherein the cascaded filters each comprises a complex filter with a pole and a zero (col. 13,line 8- col. 14, line 62).

Regarding claim 11,Vorenkamp et al discloses a filter circuit (fig. 5), comprising: a plurality of cascaded filters (510, 512 of fig. 5); wherein the cascaded filters each comprises first and second amplifiers each having a feedback loop comprising a feedback resistor and feedback capacitor coupled in parallel (col. 23,line 54- col. 24, line 67).

Regarding claim 12,Vorenkamp et al discloses a filter circuit (fig. 5), comprising: a plurality of cascaded filters (510, 512 of fig. 5); wherein at least one of the feedback resistors is programmable (col. 12, lines 7-51; col 14, lines 1-62).

Regarding claim 13,Vorenkamp et al discloses a filter circuit (fig. 5), comprising: a plurality of cascaded filters (510, 512 of fig. 5); wherein said at least one programmable feedback resistor comprises a plurality of resistors coupled in series, said plurality of resistors each having a switch coupled there across (col. 10, line 1-60; col. 11, lines 10-65).

Regarding claim 14,Vorenkamp et al discloses a filter circuit (fig. 5), comprising: a plurality of cascaded filters (510, 512 of fig. 5) wherein at least one of the feedback capacitors is Programmable (col. 12, lines 7-51; col 14, lines 1-62).

Regarding claim 15,Vorenkamp et al discloses a filter circuit (fig. 5), comprising: a plurality of cascaded filters (510, 512 of fig. 5wherein said at least one programmable feedback

capacitor comprises a plurality of capacitors coupled in parallel, said plurality of capacitors each having a switch coupled there across (col. 10, line 1-60; col. 11, lines 10-65).

Regarding claim 16, Vorenkamp et al discloses a filter circuit (fig. 5) comprising: a plurality of cascaded filters (510, 512 of fig. 5) wherein the cascaded filters each comprises a first cross coupled resistor coupled between an output of the first amplifier and an input of the second amplifier, and a second cross coupled resistor coupled between an output of the second amplifier and an input of the first amplifier (col. 21, line 42- col. 22, line 45).

Regarding claim 17, Vorenkamp et al discloses a filter circuit (fig. 5) comprising: a plurality of cascaded filters (510, 512 of fig. 5) wherein the cascaded filters each comprises a first input resistor coupled to the input of the first amplifier, and a second input resistor coupled to the input of the second amplifier (col. 21, lines 1-41; col. 21, line 42- col. 22, line45).

Regarding claim 18, Vorenkamp et al discloses a filter circuit (fig. 5) comprising: a plurality of cascaded filters (510, 512 of fig. 5) wherein the cascaded filters each comprises an input capacitor having one end coupled to the first input resistor and a second end coupled to the second input resistor (col. 21, lines 1-41).

Regarding claim 19, Vorenkamp et al discloses a filter circuit (fig. 5), comprising: a plurality of cascaded filters (510, 512 of fig. 5) wherein at least one of the capacitors is programmable (fig. 9; col. 18, line 55- col. 19, line 53).

Regarding claim 20, Vorenkamp et al discloses a filter circuit (fig. 5), comprising: a plurality of cascaded filters (510, 512 of fig. 5) wherein said at least one programmable capacitor comprises a plurality of capacitors coupled in parallel, said plurality of capacitors each having a switch coupled there across (col. 10, line 1-60; col. 11, lines 10-65).

Regarding claim 21, Vorenkamp et al discloses a filter circuit (fig. 5), comprising: a plurality of cascaded filters (510, 512 of fig. 5) wherein at least one the resistor is programmable (col. 10, line 1-60; col. 11, lines 10-65).

Regarding claim 22, Vorenkamp et al discloses a filter circuit (fig. 5), comprising: a plurality of cascaded filters (510, 512 of fig. 5) wherein said at least one programmable resistors comprises a plurality of resistors coupled in series, said plurality of resistors each having a switch coupled there across (col. 10, line 1-60; col. 11, lines 10-65).

Regarding claim 23, Vorenkamp et al discloses a filter circuit (fig. 5), comprising: a plurality of cascaded filters (510, 512 of fig. 5); and bypass means for bypassing at least one of the cascaded filters (col. 11, lines 10-65; col. 12, lines 7-51).

Regarding claim 24, Vorenkamp et al discloses a filter circuit (fig. 5), comprising: a plurality of cascaded filters (510, 512 of fig. 5); wherein the bypass means comprises a switch coupled across one of the cascaded filters (col. 11, lines 10-65; col. 12, lines 7-51).

Regarding claim 25, Vorenkamp et al discloses a filter circuit (fig. 5), comprising: a plurality of cascaded filters (510, 512 of fig. 5); wherein the bypass means comprises a plurality of switches each being coupled across a different one of the cascaded filters (col. 11, lines 10-65; col. 12, lines 7-51).

Regarding claim 26, Vorenkamp et al discloses a filter circuit (fig. 5), comprising: a plurality of cascaded filters (510, 512 of fig. 5); wherein the switches each comprises means for being individually controlled (col. 13, lines 21-65).

Regarding claim 27, Vorenkamp et al discloses a filter circuit (fig. 5), comprising: a plurality of cascaded filters (510, 512 of fig. 5) wherein the cascaded filters each comprises a biquad filter (510, 512 of fig. 5; col. 11, line 25-47; col. 27, lines 31-55).

Regarding claim 28, Vorenkamp et al discloses a filter circuit (fig. 5), comprising: a plurality of cascaded filters (510, 512 of fig. 5) wherein the cascaded filters each comprises a complex filter (col. 13,line 8- col. 14, line 62).

Regarding claim 29, Vorenkamp et al discloses a filter circuit (fig. 5), comprising: a plurality of cascaded filters (510, 512 of fig. 5) wherein the cascaded filters each comprises means for generating a pole and zero col. 12, lines 7-51; col 14, lines 1-62).

Regarding claim 30, Vorenkamp et al discloses a filter circuit (fig. 5 and fig. 19), comprising: a plurality of cascaded filters (510, 512 of fig. 5) wherein the cascaded filters each comprises a complex filter, the complex filters each comprising means for generating a pole and zero (col. 12, lines 7-51; col 14, lines 1-62).

Claims 31-43 contain similar limitations addressed in claims 1-25, and therefore are rejected under a similar rationale.

Regarding claim 44, Vorenkamp et al discloses a filter circuit (fig. 5 and fig. 19) comprising: a biquad filter (510, 512 of fig. 5; col. 11, line 25-47; col. 27, lines 31-55); and a polyphase filter coupled to the biquad filter (col. 11, lines 10-65; col. 12, lines 7-51).

Regarding claim 45, Vorenkamp et al discloses a filter circuit (fig. 5 and fig. 19) further comprising a plurality of biquad filters including the biquad filter (510, 512 of fig. 5; col. 11, line 25-47; col. 27, lines 31-55); and a plurality of polyphase filters including the polyphase filter, the

biquad filters being intertwined with the polyphase filters (col. 11,lines 10-65; col. 12, lines 7-51).

Regarding claim 46, Vorenkamp et al discloses a filter circuit (fig. 5 and fig. 19) further comprising a plurality of bypass circuits each being coupled across a different node of the biquad filters (col. 12, lines 7-51).

Regarding claim 47, Vorenkamp et al discloses a filter circuit (fig. 5 and fig. 19) wherein each of the bypass circuits are adapted for individual control. (col. 13, lines 21-65).

Claims 48-61 contain similar limitations addressed in claims 12-22, and therefore are rejected under a similar rationale.

Regarding claim 75, Vorenkamp et al discloses a method of complex filtering (fig. 5 and fig. 19) to extract a signal in a frequency spectrum comprising: a plurality of channels (col. 4, line 51- col. 5, line 45), comprising: selecting one of the channels having the signal; rejecting an image of the signal in the selected channel (col. 10, line 50- col. 11, line 65); and applying gain to the signal, the applied gain being programmable (col. 12, line 15- col. 14, line 62).

Regarding claim 76, Vorenkamp et al discloses a method of complex filtering (fig. 5 and fig. 19) to extract a signal in a frequency spectrum comprising: a plurality of channels (col. 4, line 51- col. 5, line 45) wherein the channel selection comprises tuning a center frequency of the channel (col. 13, lines 10-37; col. 14, line 5-62).

Regarding claim 77, Vorenkamp et al discloses a method of complex filtering (fig. 5 and fig. 19) to extract a signal in a frequency spectrum comprising: tuning a bandwidth of the channel (col. 9,lines 49-col. 10, line 31).

Regarding claim 78, Vorenkamp et al discloses a method of complex filtering (fig. 5 and fig. 19) to extract a signal in a frequency spectrum further comprising introducing a zero to filter a frequency in the selected channel different from a frequency of the signal (col. 13, lines 21-50).

Regarding claim 79,Vorenkamp et al discloses a method of complex filtering (fig. 5 and fig. 19) to extract a signal in a frequency spectrum comprising introducing a plurality of zeros each filtering a different frequency in the selected channel, the filtered frequencies each being different from a frequency of the signal (col. 10, line 1-60; col. 11, lines 10-65).

Regarding claim 80, Vorenkamp et al discloses a method of complex filtering (fig. 5 and fig. 19) to extract a signal in a frequency spectrum wherein the introducing of the zeros comprises programming the number of the zeros introduced (col. 12, lines 7-51; col 14, lines 1-62).

Regarding claim 81, Vorenkamp et al discloses a method of complex filtering (fig. 5 and fig. 19) to extract a signal in a frequency spectrum wherein the channel selection further comprises programming an order of complex filtering (col. 13,line 8- col. 14, line 62).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 62-74 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vorenkamp et al (US Patent No 6591091 B1) in view of Brehmer et al (US Patent No 5283484).

Regarding claims 62-74, Vorenkamp et al discloses a complex differential filter (fig 5 and fig. 19; figs. 13-14), comprising: first and second differential amplifiers each having a differential input and a differential output (col. 22,line 21-56); a first input resistor coupled to a first one of the differential inputs of the first differential amplifier (col. 23, lines 3-65; col. 24, lines 1-17); a second input resistor coupled to a second one of the differential inputs of the first differential amplifier; a third input resistor coupled to a first one of the differential inputs of the second differential amplifier (col. 24, line 19- col. 25,line 53); a fourth input resistor coupled to a second one of the differential inputs of the second differential amplifier(col. 24, line 19- col. 25,line 64); col. 29, line 1- col. 30, line 45).

However, Vorenkamp et al does not specifically disclose the feature of a first input capacitor having one end coupled to the first input resistor and another end coupled to the third input resistor; a second input capacitor having one end coupled to the second input resistor and another end coupled to the fourth input resistor; a third input capacitor having one end coupled to the third input resistor and another end coupled to the second input resistor; and
a fourth input capacitor having one end coupled to the fourth input resistor and
another end coupled to the first input resistor.

On the other hand, Brehmer et al, from the same field of endeavor, discloses in figure 1, a voltage limiter which includes a resistor receiving an input signal on a first terminal and providing an output signal on a second terminal, and a capacitor connected between the second terminal of the resistor and ground. Furthermore, Brehmer shows in figure 5, a capacitor 83 which has a first terminal connected to the second terminal of resistor 81, and a second terminal connected to the second terminal of resistor 82; and transistor 85 has a source connected to the

drain of transistor 84, a gate for receiving voltage PBIAS, and a drain connected to the second terminal of resistor 81. In addition, capacitor 105 has a first terminal connected to the second terminal of transmission gate 101, and a second terminal; capacitor 106 also has a first terminal connected to the second terminal of transmission gate 102, and a second terminal (figs. 1- 3, fig. 5; col. 1, line 58- col. 3, line 26; col. 2, line 51- col. 4, line 32; col. 5, line 24- col. 6, line 59). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the technique of Brehmer to the system of Vorenkamp in order to vary the center frequency of the filter by switching in or out the capacitors based on a four-bit binary code.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Yu-Hong US Patent No 6118984 discloses a dual conversion radio frequency transceiver.

Arevato US Patent No 6147576 discloses a method for designing filters.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Marceau Milord whose telephone number is 703-306-3023. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vivian C. Chin can be reached on 703-308-6739. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

MARCEAU MILORD

Marceau Milord
Examiner
Art Unit 2682